

App. Serial No. 10/814,426
Docket No.: 5797-00500

REMARKS

Claims 1-56 are pending in this application. Reconsideration and allowance of the application are respectfully requested.

With regard to the numbering of claims in Applicant response of June 30, 2006, Applicant appreciates the indication by the Examiner that original claims 10, 17, 41 and 52 are being considered as presented in the amended claim set of the 6/30/2006 response. The claims submitted in this response are believed to be numbered in compliance with § 1.126.

Applicant appreciates the courtesy extended by the Examiner during the telephone interview afforded on or about June 15, 2007. The substance of the interview was largely directed toward Applicant's belief that the claims are allowable for at least the reasons presented in following discussion and to the renumbering of the claims per § 1.126.

Applicant submits that the rejections are improper for failing to teach each of the claim limitations for at least the following reasons.

First, regarding the § 103(a) rejections, the Examiner's response to arguments has not addressed each of Applicant's prior arguments. More specifically, the Examiner's asserted combination does not correspond to each claim limitation even assuming *arguendo* that the cited references teach an arbiter and a mobile phone. For example, one of Applicant's previous arguments showed a lack of correspondence between the cited references and claim limitations directed toward restricting bus access in response to a change in mode. Applicant notes that merely asserting that the cited references teach a simple arbiter and mobile phone is insufficient to show correspondence to these and other claim limitations. Thus, regardless of whether or not an arbiter and a mobile phone are taught by the cited references, Applicant's previous arguments have not been addressed.

Second, regarding the 35 U.S.C. § 102(a) rejections, the Examiner has erroneously asserted that a single-bus-master system corresponds to a multiple-bus-master system and that a single-bus-master system would arbitrate requests between bus masters. More specifically, the Examiner has erroneously equated a control block for switching the current (single) master of a bus to an arbiter for handing requests between two masters.

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In the instant Office Action dated May 7, 2007, claim 1 stands rejected under 35 U.S.C. § 102(a) over Ranganathan et al. (WO 2004021684); and claims 1-31 and 38-56 stand rejected under 35 U.S.C. § 103(a) over Haartsen (U.S. Patent No. 5,842,037) in view of Hadwiger et al. (U.S. Patent No. 6,738,845).

With regard to the rejections under U.S.C. § 102(a), Applicant respectfully traverses the rejections because the teachings relied upon by the Examiner do not teach arbitrating requests between two bus masters. As shown by figure 3, the Ranganathan reference teaches that only one master is attached to the bus at any time. More specifically, block 66 shows A.P. acting as master and C.P. acting as a peripheral, while block 70 shows C.P. acting as a master, while A.P. is disabled. At no time does the Ranganathan reference teach a first master and one or more other masters are coupled to the bus. Thus, while the system may alternate which processor is the current (single) master (*i.e.*, the A.P. or the C.P.), at any specific time, the system never has more than a single master. Moreover, block 211 does not arbitrate between requests of a first bus master and another bus master because there would not be two bus masters issuing requests at the same time. Accordingly, the Ranganathan reference fails to teach correspondence to the claim limitations directed to a first master and one or more other masters being connected to the bus and to the claim limitations directed to a bus arbiter configured to arbitrate between requests from two or more bus masters.

Moreover, the Ranganathan reference does not restrict accesses to the bus in response to a mode change. Applicant respectfully submits that the Ranganathan reference merely controls which processor (A.P. or C.P.) is a bus master without restricting accesses to the bus from the respective bus master. The Ranganathan reference does not teach restricting accesses from the bus master, only switching between which processor is the bus master. Applicant submits that each of the independent claims includes limitations similar to those of claim 1, including limitations directed toward at least one of restricting access to a bus master in response to a mode change signal and/or to arbitrating between requests of at least two bus masters. For instance, claim 42 contains limitations directed towards arbitrating between requests to access the bus by the first bus master and the one or more other bus masters. Applicant respectfully submits that there is no arbitration between requests of the A.P. and C.P. processors because 1)

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the A.P. processor does not issue requests while it is de-energized and 2) the C.P. processor is not a bus master when the A.P. processor is energized.

Each claim that depends from an independent claim includes the limitations of its respective independent claim. Accordingly, Applicant respectfully submits that each of the rejections is improper and requests that they be withdrawn.

With regard to the rejections under 35 U.S.C. § 103(a), Applicant respectfully traverses the rejections. These rejections were addressed in Applicant's response of June 30, 2006, which Applicant fully incorporates herein by reference. As discussed therein, the cited combination of references does not teach "accesses by the one or more bus masters to the bus are restricted in response to a signal indicative of a change in a mode of operation of the RF circuit" as recited in claim 1. Thus, the claim limitations require that accesses by a master be restricted. The arbiter of the Hadwiger reference does not restrict accesses in response to change in a mode of operation. Thus, Applicant respectfully submits that the Examiner's asserted combination would not restrict access to the bus when a master issues an access request. Moreover, to the extent that the Examiner may be asserting that the Haarsten's interrupt routine for halting processor function corresponds to the claim limitations, Applicant respectfully submits that a system using such an interrupt routine would not restrict accesses. The Examiner appears to be confusing halting of a processor function with restricting bus accesses. During such halting, no accesses would be generated, and thus, there would be no accesses to restrict. For example, if the interrupt routine did generate an access request, the access request would be granted because neither the Haarsten nor Hadwiger references teach restrictions (responsive to a mode change) on such an access request. Thus, the rejections are improper because neither of the references teach that accesses are restricted (responsive to a mode change).

Applicant submits that each of the independent claims recite features similar to those of claim 1, including limitations directed toward at least one of restricting access to a bus master in response to a mode change signal and arbitrating between requests of at least two bus masters. Each claim that depends from an independent claim includes the limitations of its respective independent claim. Accordingly, the asserted combination

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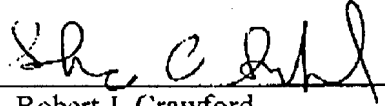
fails to teach each of the claim limitations and Applicant requests that each of the rejections be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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